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SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER
DOLAN, JENNIFER M

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,427	PAPPALARDO ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4,7-9,12-16 and 18-30 is/are rejected.

7)☒ Claim(s) 5,6,10,11 and 17 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 15 January 2002 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "auxiliary capacitor" with a "fourth transistor coupled between the first terminal of the auxiliary capacitor and a reference voltage", as well as the "phase selecting switches" must be shown or the features canceled from the claims. Additionally, the structural relationship claimed in claim 24 must be shown or the features canceled from the claims. No new matter should be entered.

2. The drawings are objected to because in figure 7, "optical stages finder" should be changed to –optimal stages finder--. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 12-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 12 recites the limitation of the presence of a "second plurality of phase selecting switches." "Phase selecting switches" were not described in the disclosure at all, and thus the disclosure is not enabling for these claims.

5. Claims 19-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Regarding claim 19, the specification and drawings fail to disclose an "auxiliary capacitor" with second and third transistors coupled between one of the pumping lines and a first terminal of the auxiliary capacitor, and with a fourth transistor coupled between the first terminal of the auxiliary capacitor and a reference voltage.

6. Claims 24 and 25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 24 recites the structural relationship that a third transistor is coupled between the input terminal and a first node of a second capacitor and a fifth transistor is coupled between the first node of the second

transistor and the reference voltage. This claim contradicts the specification, which shows that the third transistor (TP3 in 124) is connected between the input terminal and another transistor (bottommost TP transistor), but does not connect with either capacitor. Similarly, the specification shows that the fifth transistor (bottommost TP transistor) is connected between a reference voltage and the third transistor. The specification and drawings fail to show the claimed structural relationship.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 2, and 26-30 are rejected under 35 U.S.C. 102(e) as being anticipated by GB Patent Application 2,296,605 to Kim.

Regarding claim 1, Kim discloses a charge pump capable of multiple stages (figure 3), comprising: at least two pumping lines (lines for units 1B and 1C in figure 3), each line including: an input terminal for accepting an input voltage (portion connected directly to Vdd); an output terminal for delivering an output voltage (portion connecting to output, Z); a pumping capacitor (either capacitor in unit 1B or 1C) having a first terminal coupled between the input and output terminals (figure 3) and the second terminal structure to accept a phase signal (Φ);

and a switch (top transistor arrangements in 1B and 1C) coupled between the input and output terminals, the charge pump further including a switching network (N1 and N2) structured to couple the pumping lines either in a serial mode or a parallel mode depending on a state of the switching network (figure 3 and page 2).

Regarding claim 2, Kim discloses 4 stages with 2 switches in the switching network (figure 2).

Regarding claim 26, Kim discloses a method of interconnecting a set of charge pumps (1A-1D), each including phase switches and pumping capacitors, (figure 3), comprising: accepting a voltage input signal at an input terminal (Vdd), applying a series of phase signals (from Φ in figure 3) to the pumping capacitors and the phase switches to produce an output voltage at an output terminal (Z; figure 3), the output voltage different from the input voltage, and applying signals to a switching network (N1, N2) coupled between the set of charge pumps(figure 3), the signals for controlling whether the set of charge pumps should operate in a parallel or serial fashion (pages 3 and 4).

Regarding claim 27, Kim discloses applying signals to a switch coupled between two individual charge pumps (N1), including between the first and second pump, and between the second and third pump (figure 3).

Regarding claim 29, Kim discloses applying a first signal to a first transistor (N1) to cause the pumps to be serially coupled, and applying a second signal to a second transistor (N2) to cause the pumps to be coupled parallel (page 4).

Regarding claim 30, Kim discloses connecting the output signal from one charge pump to the input signal of another charge pump (figure 3).

9. Claims 18 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,369,642 to Zeng.

Zeng discloses a charge pump capable of multiple stages, having two pumping lines (figure 4), each line including: an input terminal (Vcc) for accepting an input voltage; an output terminal (Vout) for delivering an output voltage, the output voltage different than the input voltage; a pumping capacitor (C1b, C2b, etc.) having a first terminal coupled between the input and output terminals (figure 4), and a second terminal structured to accept a phase signal (CLK 1), and a switched diode (formed from T1a, T1b and C1a) coupled between the input terminal and the output terminal and structured to disrupt a connection between the terminals when activated by a switching signal (figure 4); the charge pump further including: a switching network (36) coupled between the pumping lines and structure to couple the pumping lines in a serial or parallel mode depending on a state of the switching network (see figures 3 and 4). Zeng further discloses an output switched diode (formed from T17 and C10) coupled to the output terminal (figure 4).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-4, 7, and 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,767,735 to Javanifard et al. in view of U.S. Patent No. 6,504,422 to Rader et al.

Regarding claim 1, Javanifard discloses a charge pump capable of having multiple stages (see column 4, line 60 – column 5, line 55), comprising: at least two pumping lines (figure 3; each line containing a charge pump unit), each line including: an input terminal (portion connected to Vpp line) for accepting an input voltage; an output terminal (portion connected to memory 390) for delivering an output voltage, and a charge pump unit (310, 320,etc.). Javanifard further discloses a switching network (switches in figure 3) structured to couple the pumping lines either in a serial mode or a parallel mode, depending on the state of the switching network (see table 1).

Javanifard fails to disclose the specific device arrangement for each of the charge pump units.

Rader et al. discloses a charge pump unit (figure 2) having a pumping capacitor (C1) having a first terminal (+ terminal) coupled between the input and output terminals, and having a second terminal structured to accept a phase signal (figures 2 and 3), and a switch (S2, S4) coupled between the input terminal and the output terminal and structured to disrupt a connection between the terminals when activated by a switching signal.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the charge pump unit (310) of Javanifard is structured identically to the charge pump unit taught by Rader. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide a charge pump unit

structured like that of Rader, because the charge pump unit of Rader can act as a 1x, 1.5x, 2x, or 3x voltage multiplier, which increases the versatility and controllability of the output voltage (see Rader, column 3, lines 30 – 52).

Regarding claim 2, Javanifard discloses twelve pumping lines and a switching network with two switches (figure 3).

Regarding claim 3, Javanifard discloses that some switches in the switching network are structured to remain open during a charge pumping operation (table 1, figure 3).

Javanifard fails to disclose that some switches in the pumping lines are structured to remain open during a charge pumping operation.

Rader discloses that some switches in the pumping lines are structured to remain open during a charge pumping operation (figure 3; table 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that some of the switches in the pumping lines of Rader as modified by Javanifard, in claim 1, supra, are structured to remain open during charge pumping, as is further taught Rader. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to specify that some switches in the pumping lines are structured to remain open, because Rader shows that in order to achieve the 1x, 1.5x, 2x, and 3x voltage multiplication, various switches must be fixed open or closed depending on the preferred multiplication mode (see Rader, column 3, line 30-67).

Regarding claim 4, Javanifard discloses an optimal stages finder coupled to the switching network (column 5, lines 58-67; column 7, lines 10-42).

Regarding claim 7, Javanifard discloses a comparison circuit structured to compare a reference voltage to a power supply voltage and generate an output signal (column 7, lines 52-57

Regarding claim 12, Javanifard discloses a variable stage charge pump, comprising: a plurality of units (310, 320, etc.), each unit including an input terminal (terminal connected to Vpp in figure 3) and an output terminal (terminal connected to flash memory in figure 3) of a charge pump unit. Javanifard further discloses a plurality of switches (switches connecting unit 310 to unit 320, etc. in figure 3) coupled to one of the terminals of one of the units and structured to be coupled to one of the terminals in another unit (figure 3).

Javanifard is silent as to the internal structure of the charge pump unit.

Rader discloses a charge pump unit (figure 2) having a first switch (S4) coupled between the input terminal and a first terminal of a first capacitor (C1), a second switch (S2) coupled between the input terminal and a first terminal of a second capacitor (C2), the second terminal of the first and second capacitors for receiving a pumping signal (figures 2 and 3); a third switch (S5) coupled between the first terminals of the first and second capacitors; a fourth switch (S9) coupled between the first terminal of the first capacitor and the output terminal, and a fifth switch (S10) coupled between the first terminal of the second capacitor and the output terminal. Rader further teaches that both the first and second capacitors are coupled to both the input and output terminals.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the charge pump unit of Javanifard is structured identically to the charge pump unit taught by Rader. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide a charge pump unit

structured like that of Rader, because the charge pump unit of Rader can act as a 1x, 1.5x, 2x, or 3x voltage multiplier, which increases the versatility and controllability of the output voltage (see Rader, column 3, lines 30 – 52). It is noted that by using the charge pump unit of Rader, the plurality of switches of Javanifard would end up coupled to one of the capacitors in one of the units and one in another unit, since both the capacitors of Rader and the switches of Javanifard are connected to the output terminal.

Regarding claim 13, Rader discloses two units, with the phase selecting switch coupled between the output terminal of the first unit and the input terminal of the second unit (figure 1). Since the variable stage charge pump of Javanifard as modified by Rader, in claim 12, supra, has the first terminal of the first capacitor of each unit connected to both the input and output terminals, the limitations of the claim are automatically met.

Regarding claim 14, Rader discloses that the number of phase selecting switches is one less than the number of units (figure 3).

Regarding claim 15, Rader implicitly discloses 3 units (figure 3) with phase selecting switches connecting the output terminal of the first unit to the input terminal of the second, and the output terminal of the second to the input terminal of the third. Since the variable stage charge pump of Javanifard as modified by Rader, in claim 12, supra, has the first terminal of the first and second capacitors of each unit connected to both the input and output terminals (see Rader, figure 2), the limitations of the claim are automatically met.

Regarding claim 16, Javanifard discloses an optimal stages finder coupled to the switching network (column 5, lines 58-67; column 7, lines 10-42).

12. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Javanifard et al. in view of Rader et al. as applied to claim 7 above, and further in view of U.S. Patent No. 6,150,835 to Hazen et al.

Javanifard is silent as to the nature of the comparison circuit.

Hazen discloses a comparison circuit comprising: a resistor ladder (502 and 504) coupled to the power supply voltage (410; figure 5), two reference voltages (532 and 531), and a set of comparators (505 and 507). Hazen further teaches that the inputs of the comparators are coupled to the resistor ladders and reference voltages (figure 5), and the outputs are coupled to a signal latching circuit (figure 5).

Hazen fails to disclose a second resistor ladder.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the comparison circuit of Javanifard as modified by Rader, such that it includes the resistor ladder and comparators, as taught by Hazen, and such that it further includes a second resistor ladder. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide the comparison circuit taught by Hazen, because Hazen shows that the circuit accurately checks the range into which the voltage falls, and applies the appropriate signals to the charge pump in light of the detected signal (Hazen, column 4, line 45- column 5, line 55). A person having ordinary skill would additionally have been motivated to provide a second resistor ladder, because the second resistor ladder would act as a voltage divider, such that the 2V and 1V reference signals could be provided using the same supplied reference voltage, rather than requiring two separate voltages to be applied, as is appreciated by one skilled in the art.

Allowable Subject Matter

13. Claims 5, 6, 10, 11, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record, considered as a whole, fails to suggest a phase assigner coupled to the optimal stages finder and comprising a plurality of multiplexing circuits for a variable stage charge pump, as in claims 5, 6, and 17, as well as a signal latching circuit with a logic circuit and latches, as in claims 10 and 11.

The closest art of record includes the publications listed supra in the rejection. None of these references included these claimed features for determining the number of stages. The use of the multiplexing circuit allows the switches and capacitors in the charge pump to be controlled, such that the required number of charge pump units and stages are used. Additionally, the use of the signal latching circuit as specified allows for the optimal number of stages to be directly outputted and implemented into the switch control structure.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,483,434 to Seesink discloses a voltage comparator for a charge pump.

b. U.S. Patent Publication No. 2002/0130701 to Kleveland discloses a charge pump in which selected stages can be activated.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (703) 305-3233. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd
May 23, 2003

Carl Whitehead
CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800